UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/760,501 | 01/21/2004 | Akira Nishiyama | 247959US2TTCRD | 1483 |

22850 7590 01/10/2006

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

| EXAMINER | |
|---|---|
| WARREN, MATTHEW E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/760,501 | NISHIYAMA ET AL | |
| | Examiner | Art Unit | |
| | Matthew E. Warren | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the Amendment filed on October 14, 2005.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 7-10, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horikawa (US Pub 2002/0135030 A1) in view of Shirahata et al. (US 6,525,380).

In re claim 1, Horikawa shows (fig. 1) a complementary field effect transistor comprising; a semiconductor substrate (2); an n-type field effect transistor (10) provided on the semiconductor substrate having: a first gate insulating film (14) containing an oxide ($TiO_2$, $ZrO_2$, or $HfO_2$) including an element selected from the group consisting group IV metals and Lanthanoid metals [0062-0063] (such as Ti, Zr, or Hf); a first gate electrode (15) provided on the first gate insulating film; and n-type source and drain regions (12, 13) formed on both sides of the first gate electrode; and p-type field effect transistor (30) provided on the semiconductor substrate having: a second gate insulating film (34) containing an oxide ($TiO_2$, $ZrO_2$, or $HfO_2$) including an element

selected from the group consisting group IV metals and Lanthanoid metals [0062-0063] (such as Ti, Zr, or Hf); a second gate electrode (35) provided on the second gate insulating film; p-type source and drain regions (32, 33) provided on both sides of the second gate electrode. Horikawa shows all of the elements of the claims except the first gate insulating film further containing boron and the second gate insulating film containing no boron. Shirahata et al. shows (fig. 15) a CMOS device having first and second gates. The first gate insulation film (5 on the right) contains boron to trap charge (14) within the insulator while the second gate insulation film (5 on the left) contains no boron (col. 7, line 61-col. 8, line 4). With this configuration, a surface channel FET can be formed having a lower threshold voltage (Vth) (col. 8, lines 10-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CMOS device of Horikawa by adding boron to the gate insulating film of one of the gates as taught by Shirahata to lower the threshold voltage of the device.

In re claims 2 and 3, Horikawa discloses that [0057] a main component of the first gate electrode and a main component of the second gate electrode are the same and that the gate electrodes consist of one of Pt, Cu, Pd, Co, and W.

In re claim 5, Horikawa discloses [0078-0080] that the first gate insulating film includes positive charge.

In re claim 7, Horikawa discloses [0057] that the first gate electrode includes the group III element (Al).

In re claim 8, Horikawa et al. shows (fig. 1) a complementary field effect transistor comprising: semiconductor substrate (2); an n-type field effect transistor (10) provided on the semiconductor substrate having: a first gate insulating film (14) containing an oxide ($TiO_2$, $ZrO_2$, or $HfO_2$) including an element selected from the group consisting of group IV metals and Lanthanoid metals [0062-0063] (such as Ti, Zr, or Hf); a first gate electrode (15) provided on first gate insulating film; and n-type source and drain regions (12 and 13) formed on both sides of the first gate electrode; and a p-type field effect transistor (30) provided on the semiconductor substrate having: second gate insulating film (34) containing an oxide ($TiO_2$, $ZrO_2$, or $HfO_2$) including an element selected from the group consisting of group IV elements and Lanthanoid metals (such as Ti, Zr, or Hf); a second gate electrode (35) provided on the second gate insulating film; and p-type source and drain regions (32, 33) provided on both sides of the second gate electrode. Horikawa shows all of the elements of the claims except the first gate insulating film further containing no boron and the second gate insulating film containing boron. Shirahata et al. shows (fig. 15) a CMOS device having first and second gates. The first gate insulation film (5 on the right) contains boron to trap charge (14) within the insulator while the second gate insulation film (5 on the left) contains no boron (col. 7, line 61-col. 8, line 4). With this configuration, a surface channel FET can be formed having a lower threshold voltage (Vth) (col. 8, lines 10-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CMOS device of Horikawa by adding boron to the gate insulating film of one of the gates as taught by Shirahata to lower the threshold voltage of the device.

In re claims 9 and 10, Horikawa discloses that [0057] a main component of the first gate electrode and a main component of the second gate electrode are the same and that the gate electrodes consist of one of Pt, Cu, Pd, Co, and W.

In re claim 12, Horikawa discloses [0078-0080] that the second gate insulating film includes negative charge.

In re claim 14, Horikawa discloses [0057] that the second gate electrode includes the group V element or aluminum.

Claims 4, 6, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horikawa (US Pub 2002/0135030 A1) in view of Shirahata et al. (US 6,525,380)as applied to claims 1, 5, 8, and 12 above, and further in view of Wallace et al. (US 6,020,243).

In re claims 4, 6, 11, and 13, Horikawa and Shirahata show all of the elements of the claims except the concentration of the compound, and the positive or negative charge in the first or second gate insulating film is higher on side of the first gate electrode than on a side of the semiconductor substrate. Wallace et al. discloses (col. 2, lines 27-60) a high-k dielectric of zirconium or hafnium silicon oxynitride where most of the metal dopant is deposited in the upper surface of the oxide and near the gate electrode to employ primarily Si/SiO bonding at the silicon surface with resulting low interface state densities. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate insulating film of Horikawa in view of Shirahata by primarily doping the upper portions of the gate

insulating film on the side of the gate electrode as taught by Wallace to form the gate insulating film having low interface state densities and good bonding with the substrate surface.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Koyama et al. (US Pub. 2003/0122199 A1) discloses CMOS devices having metallic compounds that include boron and are formed in the gate structure. King et al. (US 6,680,245 B1) discloses that boron is added to gate oxide to trap charges.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
January 5, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER